WE CLAIM:

1. A method for enabling fast clock phase locking in a phase-locked loop, the phase-locked loop including a phase detector for receiving an input digital signal associated with a rewritable digital versatile disc and an input phase-locking clock signal, and a voltage controlled oscillator that generates an oscillator output, said method comprising the steps of:

(a) in response to the oscillator output, obtaining multiple sampling points of the input digital signal, wherein temporally adjacent ones of the sampling points are spaced apart from each other by an interval;

(b) comparing logic levels of each temporally adjacent pair of the sampling points to detect presence of a logic level transition in the input digital signal; and

(c) providing an adjusted input phase-locking clock signal for replacing a current input phase-locking clock signal to the phase detector, the adjusted input phase-locking clock signal corresponding to one of the sampling points in the temporally adjacent pair that was detected to have the logic level transition occurring in the interval of the temporally adjacent pair.

2. The method as claimed in Claim 1, wherein step (a) includes:

generating a number (N) of sampling clock signals having the same clock frequency and different clock

phases, each of the sampling clock signals forming a relative phase difference equal to 360/N degrees with another one of the sampling clock signals; and

sampling the input digital signal at clock edges of the sampling clock signals to obtain the sampling points.

3. The method as claimed in Claim 2, wherein, in step (c), the adjusted input phase-locking clock signal is selected from one of the sampling clock signals which has one of the clock edges thereof defining the interval that was detected to have the logic level transition occurring therein.

4. The method as claimed in Claim 1, wherein the logic level transition is a transition from one of high and low logic states to the other of the high and low logic states.

5. A method for enabling fast clock phase locking in a phase-locked loop, the phase-locked loop including a phase detector for receiving an input digital signal associated with a rewritable digital versatile disc and an input phase-locking clock signal, and a voltage controlled oscillator that generates an oscillator output, said method comprising the steps of:

in response to the oscillator output, generating a number (N) of sampling clock signals;

sampling the input digital signal at clock edges of the sampling clock signals to obtain multiple sampling points of the input digital signal, wherein temporally

adjacent ones of the sampling points are spaced apart from each other by an interval;

comparing logic levels of each temporally adjacent pair of the sampling points to detect presence of a logic level transition in the input digital signal; and

selecting one of the sampling clock signals that is to be provided to the phase detector as the input phase-locking clock signal, the selected one of the sampling clock signals having one of the clock edges thereof defining the interval that was detected to have occurrence of the logic level transition in the input digital signal.

6. The method as claimed in Claim 5, wherein the sampling clock signals have the same clock frequency and different clock phases, each of the sampling clock signals forming a relative phase difference equal to 360/N degrees with another one of the sampling clock signals.

7. The method as claimed in Claim 5, wherein the logic level transition is a transition from one of high and low logic states to the other of the high and low logic states.

8. An apparatus for enabling fast clock phase locking in a phase-locked loop, the phase-locked loop including a phase detector for receiving an input digital signal associated with a rewritable digital versatile disc and an input phase-locking clock signal, and a voltage controlled oscillator that generates an oscillator

output, said apparatus comprising:

a sampling clock generator adapted to receive the oscillator output from the voltage controlled oscillator, said sampling clock generator generating a number (N) of sampling clock signals in response to the oscillator output;

a detector unit coupled to said sampling clock generator and adapted to receive the input digital signal, said detector unit sampling the input digital signal at clock edges of the sampling clock signals to obtain multiple sampling points of the input digital signal, wherein temporally adjacent ones of the sampling points are spaced apart from each other by an interval;

said detector unit comparing logic levels of each temporally adjacent pair of the sampling points to detect presence of a logic level transition in the input digital signal; and

a selector unit coupled to said sampling clock generator and said detector unit, said selector unit being controlled by said detector unit to select one of the sampling clock signals from said sampling clock generator, wherein the selected one of the sampling clock signals has one of the clock edges thereof defining the interval that was detected by said detector unit to have occurrence of the logic level transition in the input digital signal, said selector unit being adapted to provide the selected one of the sampling clock signals

to the phase detector as the input phase-locking clock signal.

9. The apparatus as claimed in Claim 8, wherein the sampling clock signals generated by said sampling clock generator have the same clock frequency and different clock phases, each of the sampling clock signals forming a relative phase difference equal to 360/N degrees with another one of the sampling clock signals.

10. The apparatus as claimed in Claim 8, wherein the logic level transition is a transition from one of high and low logic states to the other of the high and low logic states.

11. The apparatus as claimed in Claim 8, wherein said detector unit includes a signal processing circuit, said signal processing circuit including:

a sampling circuit for sampling the input digital signal at the clock edges of the sampling clock signals; and

a comparison circuit coupled to said sampling circuit for comparing logic levels of each temporally adjacent pair of the sampling points.

12. The apparatus as claimed in Claim 11, wherein said sampling circuit is constructed from flip-flops.

13. The apparatus as claimed in Claim 12, wherein the flip-flops are D-type flip-flops.

14. The apparatus as claimed in Claim 11, wherein said comparison circuit is constructed from exclusive-OR

logic gates.

15. The apparatus as claimed in Claim 11, wherein said detector unit further includes a delay circuit coupled to and disposed between said sampling clock generator and said signal processing circuit.